AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A clock generating apparatus comprising:

a first phase lock loop device to be powered by a first power supply voltage; and

a second phase lock loop device, coupled to the first phase lock loop device, to be powered by the first power supply voltage and a second power supply voltage, the second phase lock loop device to output a clock signal having an adaptive frequency based on the second power supply voltage.

2. (Original) The clock generating apparatus of claim 1, wherein the first power supply voltage comprises an analog voltage and the second power supply voltage comprises a digital voltage.

3. (Original) The clock generating apparatus of claim 1, wherein fluctuations of the frequency of the clock signal output from the second phase lock loop device are based on fluctuations of the second power supply voltage.

4. (Original) The clock generating apparatus of claim 1, wherein the first phase lock loop device outputs a clock signal having a fixed frequency, the clock signal having the fixed frequency being input to the second phase lock loop device.

5. (Original) The clock generating apparatus of claim 1, wherein the second phase lock loop device includes components powered by the first power supply voltage and components powered by the second power supply voltage.

6. (Original) The clock generating apparatus of claim 5, wherein the second phase lock loop device includes a voltage controlled oscillator (VCO) powered by the second power supply voltage.

7. (Original) The clock generating apparatus of claim 6, wherein a sensitivity to droop is based on a coupling percentage of the second power supply voltage to power the VCO.

8. (Original) The clock generating apparatus of claim 1, wherein a sensitivity to voltage droop is determined based on a ratio of capacitor sizes within the second phase lock loop device.

9. (Original) The clock generating apparatus of claim 1, wherein a sensitivity to voltage droop is determined based on a ratio of transistor sizes within the second phase lock loop device.

10. (Original) The clock generating apparatus of claim 1, wherein the apparatus corrects for phase error accumulation.

11. (Original) The clock generating apparatus of claim 1, further comprising buffers to couple core components, operating based on the clock signal, with external I/O.

12. (Original) A clocking system comprising:

an adaptive phase lock loop device powered by an analog power supply voltage and a digital power supply voltage, the adaptive phase lock loop device to receive a first clock signal and to output a second clock signal having an adaptive frequency based on a voltage of the digital power supply voltage.

13. (Original) The clocking system of claim 12, further comprising a fixed phase lock loop device powered by the analog power supply voltage, the fixed phase lock loop device to receive a reference clock signal and to provide the first clock signal to the adaptive phase lock loop device.

14. (Original) The clocking system of claim 13, wherein fluctuations of the frequency of the second clock signal are based on fluctuations of the digital power supply voltage.

15. (Original) The clocking system of claim 13, wherein the fixed phase lock loop device outputs the first clock signal having a fixed frequency.

16. (Original) The clocking system of claim 12, wherein the adaptive phase lock loop device includes components powered by the analog power supply voltage and components powered by the digital power supply voltage.

17. (Original) The clocking system of claim 16, wherein the adaptive phase lock loop device includes a voltage controlled oscillator (VCO) powered by the digital power supply voltage.

18. (Original) The clocking system of claim 17, wherein a sensitivity to droop is based on a coupling percentage of the second power supply voltage to power the VCO.

19. (Original) The clocking system of claim 12, wherein a sensitivity to voltage droop is determined based on a ratio of capacitor sizes within the adaptive phase lock loop device.

20. (Original) The clocking system of claim 12, wherein a sensitivity to voltage droop is determined based on a ratio of transistor sizes within the adaptive phase lock loop device.

21. (Original) The clocking system of claim 12, further comprising buffers to couple core components with external I/O.

22. (Original) An electronic system comprising:

an integrated circuit having a clock generating apparatus; and

I/O components coupled external to the integrated circuit, wherein the clock generating apparatus comprises:

a first phase lock loop device to be powered by a first power supply voltage; and

a second phase lock loop device to be powered by the first power supply voltage and a second power supply voltage, the second phase lock loop device to output a clock signal having a frequency based on the second power supply voltage.

23. (Original) The electronic system of claim 22, wherein the first power supply voltage comprises an analog voltage and the second power supply voltage comprises a digital voltage.

24. (Original) The electronic system of claim 22, wherein fluctuations of the frequency of the clock signal output from the second phase lock loop device are based on fluctuations of the second power supply voltage.

25. (Original) The electronic system of claim 22, further comprising buffers to couple core components of the integrated circuit with the I/O components.

26. (Original) The electronic system of claim 22, wherein the first power supply and the second power supply are external to the integrated circuit.

27. (New) The electronic system of claim 22, wherein the first power supply voltage is different than the second power supply voltage.

28. (New) The electronic system of claim 1, wherein the first phase lock loop device includes a first bias circuit and a first voltage controlled oscillator, the first bias circuit to provide a bias voltage to the first voltage controlled oscillator, the bias voltage being different than the first and second power supply voltages.

29. (New) The electronic system of claim 28, wherein the second phase lock loop device includes a second bias circuit and a second voltage controlled oscillator, the second bias

circuit to provide a bias voltage to the second voltage controlled oscillator, the bias voltage being different than the first and second power supply voltages.

30. (New) The electronic system of claim 22, further comprising a multiplexer to select an output of the first phase lock loop device or to select the clock signal output from the second phase lock loop device.

31. (New) The clock generating apparatus of claim 1, wherein the first power supply voltage is different than the second power supply voltage.

32. (New) The clock generating apparatus of claim 1, further comprising a multiplexer to select an output of the first phase lock loop device or to select the clock signal output from the second phase lock loop device.

33. (New) The clock generating apparatus of claim 1, wherein the first phase lock loop device includes a first bias circuit and a first voltage controlled oscillator, the first bias circuit to provide a bias voltage to the first voltage controlled oscillator, the bias voltage being different than the first and second power supply voltages.

34. (New) The clock generating apparatus of claim 33, wherein the second phase lock loop device includes a second bias circuit and a second voltage controlled oscillator, the second

bias circuit to provide a bias voltage to the second voltage controlled oscillator, the bias voltage being different than the first and second power supply voltages.